

# Taimur Rabuske

Analog and mixed-signal integrated circuit design · data converters, clocking, power and high-speed links · architecture to silicon

[taimur.rabuske@gmail.com](mailto:taimur.rabuske@gmail.com) · Wilmington, Massachusetts, USA · [LinkedIn](#) · [Google Scholar](#)

---

## PROFILE

---

Analog and mixed-signal IC designer with a PhD in microelectronics and more than fifteen years in CMOS silicon, currently at Analog Devices. I own subsystems end to end — feasibility study and architecture exploration, specification derivation, transistor-level design, verification, layout sign-off, tape-out and bench validation — across data converters, clocking, power management and high-speed links. Silicon in eight process generations, from 0.5  $\mu\text{m}$  bulk CMOS to 5 nm FinFET. An MSc in computer science sits alongside the microelectronics: I write Python for modelling, optimisation, test automation and in-house EDA tooling, and I have supervised doctoral and MSc researchers, written funded proposals, and designed circuits for industry partners' commercial products.

### OWNERSHIP

#### **Subsystems, not just blocks**

At Analog Devices I take subsystems from feasibility study and architecture exploration through implementation, verification and validation, and on into the lab with the silicon measurement team. Every one has been a new architecture rather than a port of existing IP; six patent applications are under examination on the results.

### BREADTH

#### **Converters, clocks, power and links**

SAR, charge-sharing,  $\Sigma\Delta$  and high-speed flash ADCs; clock synthesis and LC, ring, relaxation and injection-locked oscillators; LDOs with wideband PSR, references and biasing; a die-to-die SerDes link; and sensor and biomedical front-ends.

### SILICON

#### **Eight process generations**

Prototypes and products taped out from 0.5  $\mu\text{m}$  to 5 nm, in bulk CMOS, SOI and FinFET. On the research prototypes I ran the whole path myself — specification, architecture, schematic, custom layout, DRC/LVS sign-off, tape-out, PCB, firmware and bench characterisation.

### SYSTEMS

#### **Specs that reach past the die**

Derived the specifications for complete instruments, not only the chip: partitioning between silicon, board and software, then the boards, drivers and measurement software that had to exist around it for the prototype to prove anything.

## SOFTWARE

### **An MSc in computer science, and Python everywhere**

Behavioural modelling, gm/ID sizing, simulation-driven optimisation, test automation and bench data analysis. Published in-house EDA tooling: PyCO, a parallel genetic-algorithm optimiser for analog circuits, and Polymath, a platform for rapid development of modular EDA tools.

## LEADERSHIP

### **Research led, researchers grown**

Led analog and mixed-signal circuit research at INESC-ID: supervised six doctoral and six MSc researchers, wrote the proposals that funded the work, sat on the Scientific Council, and designed circuits for industry partners' commercial products under collaboration agreements.

## APPOINTMENTS

---

2023 – Present

### **Analog/Mixed-Signal Design Engineer**

Analog Devices · Wilmington, Massachusetts

- Own analog and mixed-signal subsystems across the full flow: feasibility study, architecture exploration and specification, transistor-level implementation, verification, validation, and support to the silicon measurement team through bring-up.
- Delivered LDOs, clock-synthesis circuits, a die-to-die SerDes link and an audio  $\Sigma\Delta$  ADC, alongside the converter cores, sampling networks, comparators, references and biasing around them.
- Each subsystem was a new architecture rather than a port of existing IP; six patent applications are currently under examination.
- Advanced-node work in FinFET and SOI, including noise, matching, settling and jitter budgets for high-resolution converters and the clocking that feeds them.

2016 – 2023

### **Senior Researcher**

INESC-ID · Lisbon, Portugal

- Led the analog and mixed-signal circuit research line: low-voltage low-power SAR and charge-sharing ADCs,  $\Sigma\Delta$  modulators, dynamic comparators and calibration, oscillators and clock generation, and biomedical and sensor front-ends.
- Ran the whole silicon path on research prototypes – specification, architecture, schematic, custom layout, DRC/LVS sign-off, tape-out, PCB, firmware and bench characterisation – in processes from 0.35  $\mu\text{m}$  to 40 nm.
- Set system-level specifications that reached past the die, partitioning a product between silicon, board and software and then specifying the boards, drivers and measurement software around it.
- Technical lead on biomedical and industrial programmes – magnetic cytometry, smart catheters, implant hermeticity monitoring and magnetoresistive non-destructive testing – and on industry collaborations in which I designed circuits for commercial products.
- Supervised and co-supervised six doctoral and six MSc researchers, and wrote the project proposals that funded the group's work.
- Member of the Scientific Council, 2017 – 2023: institutional research strategy and internal review.

2010 – 2016

### **Research Assistant**

INESC-ID · Lisbon, Portugal

Doctoral and pre-doctoral work on charge-sharing SAR ADCs: architecture analysis, MOSCAP-based DACs, comparator offset auto-zeroing and self-timed SAR control, validated in four fabricated prototypes.

2018

### **Visiting Scholar**

Delft University of Technology · Delft, Netherlands

2009

### **Intern Researcher**

Gwangju Institute of Science & Technology · Gwangju, South Korea

A semester in South Korea on energy-efficient SAR ADCs, the work that became my first published converter.

## **EDUCATION**

---

2012 – 2016

### **PhD, Electrical and Computer Engineering (with honors)**

Instituto Superior Técnico, Universidade de Lisboa

Microelectronics. Thesis on charge-sharing SAR ADCs for low-voltage low-power applications, later published as a Springer monograph. Awarded with distinction and honour.

2010 – 2011

### **MSc, Computer Science**

Universidade Federal de Santa Maria, Brazil

Thesis on techniques for power reduction in SAR ADCs. The first half read in Brazil, the second carried out at INESC-ID in Lisbon.

2005 – 2009

### **BSc, Electrical Engineering**

Universidade Federal de Santa Maria, Brazil

Including an exchange semester at the Gwangju Institute of Science and Technology, South Korea.

## **EXPERTISE**

---

### **CIRCUITS**

- SAR, charge-sharing, charge-redistribution,  $\Sigma\Delta$  and high-speed flash data converters
- Clock synthesis, and LC, ring, relaxation and injection-locked oscillators
- LDOs with wideband PSR, references, biasing and reference buffers
- Die-to-die SerDes serialisers and deserialisers, and high-speed links
- Dynamic comparators and latches, with background offset and noise calibration
- Biomedical and sensor front-ends: magnetoresistive, chopper, instrumentation, VGA
- Continuous-time filters, track-and-hold, bootstrapped switches and sampling networks
- Energy harvesting and wireless links for implants; multi-valued CMOS logic

## DESIGN FLOW

- Feasibility study, architecture exploration and specification derivation
- Behavioural modelling; noise, offset, matching, settling and jitter analysis
- PVT, corner and Monte Carlo verification; PSS, PXF and PNOISE for comparators
- Custom layout, DRC/LVS/PEX sign-off, tape-out, bring-up and bench characterisation
- Low-voltage, low-power CMOS, down to 0.35 V supplies
- Background and foreground self-calibration
- Top-level integration and pad ring
- Digital when a block needs it – SystemVerilog RTL, synthesis, place-and-route and sign-off

## SOFTWARE & TOOLS

- Cadence Virtuoso, Spectre and the analog verification flow; HSPICE
- Python for modelling, sizing, optimisation, test automation and data analysis
- In-house EDA tooling: gm/ID sizing, genetic-algorithm optimisation, modular EDA platforms
- Static and dynamic converter characterisation on the bench
- PCB design, instrument control and firmware for prototype test benches
- Version control and continuous integration for analog and mixed-signal teams

## LANGUAGES

- English – fluent
- Portuguese – native

## SILICON

---

Chips taped out across eight process generations, in bulk CMOS, SOI and FinFET – research prototypes I designed and characterised end to end, and production subsystems at Analog Devices.

0.5  $\mu\text{m}$  0.35  $\mu\text{m}$  0.18  $\mu\text{m}$  0.13  $\mu\text{m}$  65 nm 40 nm 22 nm 5 nm

## BOOKS

---

MONOGRAPH · SPRINGER

### **Charge-Sharing SAR ADCs for Low-Voltage Low-Power Applications**

T. Rabuske and J. Fernandes · Analog Circuits and Signal Processing series · Springer, Cham, 2017 · [doi](#)

A full treatment of the charge-sharing SAR topology: the mechanisms that limit its performance – capacitor mismatch, comparator offset and noise – with closed-form analysis, mitigation techniques, and four fabricated prototypes operating from 0.35 V to 0.6 V.

1. T. Rabuske, Conversores A/D SAR por Entrelaçamento no Tempo em Tecnologia CMOS 130 nm (in Portuguese). Novas Edições Acadêmicas, 2016.
2. J. Silva, D. Oliveira, D. M. Caetano, T. Rabuske and J. Fernandes, “Variable Bandwidth Chopper Amplifier for Eddy-Current Non-Destructive Testing,” book chapter, 2017. DOI 10.3233/978-1-61499-767-2-187. · [doi](#)

1. **A 0.3-mm<sup>2</sup> 1.3  $\mu$ W Wireless Monitoring System IC for Hermeticity Testing of Biomedical Implants**  
G. Rodrigues, **T. Rabuske** and J. Fernandes · *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 72, no. 8, pp. 3911–3923, 2025 · [doi](#)
2. **Integrated Circuit for Magnetic Encoder Sensing in TMR-Based Industrial Positioning System**  
J. Silva, D. M. Caetano, **T. Rabuske**, S. Cardoso, M. Piedade and J. Fernandes · *IEEE Transactions on Industrial Electronics*, vol. 71, no. 8, pp. 9904–9913, 2024 · [doi](#)
3. **Maximizing Energy Harvesting in a Miniaturized Implant With an Integrated Coil Receiver**  
G. Rodrigues, J. Silva, H. I. Busse, D. M. Caetano, J. Fernandes and **T. Rabuske** · *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 70, no. 10, pp. 3762–3766, 2023 · [doi](#)
4. **Artificial Neural Networks for GMR-Based Magnetic Cytometry**  
D. M. Caetano, R. Afonso, A. R. Soares, J. Silva, H. I. Busse, V. Silvério, **T. Rabuske**, G. N. Tavares, J. Fernandes and S. Cardoso · *IEEE Transactions on Instrumentation and Measurement*, vol. 72, pp. 1–11, 2023 · [doi](#)
5. **Calibrating Amplifiers Nonlinearity Using Comparator-Based ADCs**  
F. A. Rabuske, **T. Rabuske**, S. Liu and J. Fernandes · *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 67, no. 3, pp. 435–439, 2020 · [doi](#)
6. **High-Resolution Nondestructive Test Probes Based on Magnetoresistive Sensors**  
D. M. Caetano, **T. Rabuske**, J. Fernandes, M. Pelkner, C. Fermon, S. Cardoso, B. Ribes, F. Franco, J. Paul, M. S. Piedade and P. P. Freitas · *IEEE Transactions on Industrial Electronics*, vol. 66, no. 9, pp. 7326–7337, 2019 · [doi](#)
7. **Analysis and Background Self-Calibration of Comparator Offset in Loop-Unrolled SAR ADCs**  
S. Liu, **T. Rabuske**, J. Paramesh, L. Pileggi and J. Fernandes · *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 65, no. 2, pp. 458–470, 2018 · [doi](#)
8. **A 5-bit 300–900-MS/s 0.8–1.2-V Supply Voltage ADC With Background Self-Calibration**  
F. A. Rabuske, **T. Rabuske** and J. Fernandes · *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 64, no. 1, pp. 1–5, 2017 · [doi](#)
9. **Effect of Comparator Offset on the Linearity of Charge Sharing ADCs**  
**T. Rabuske** and J. Fernandes · *Analog Integrated Circuits and Signal Processing*, vol. 90, no. 1, pp. 9–16, 2017 · [doi](#)
10. **A 2.4 GHz high-performance CMOS differential quadrature relaxation oscillator**  
E. Ortigueira, **T. Rabuske**, L. B. Oliveira, J. Fernandes and M. M. Silva · *Analog Integrated Circuits and Signal Processing*, vol. 90, no. 1, 2017 · [doi](#)
11. **A SAR ADC With a MOSCAP-DAC**  
**T. Rabuske** and J. Fernandes · *IEEE Journal of Solid-State Circuits*, vol. 51, no. 6, pp. 1410–1422, 2016. Most-downloaded JSSC paper, June 2016 · [doi](#)
12. **An 8-bit 0.35-V 5.04-fJ/conversion-step SAR ADC With Background Self-Calibration of Comparator Offset**  
**T. Rabuske**, F. A. Rabuske, J. Fernandes and C. Rodrigues · *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 23, no. 7, pp. 1301–1307, 2015 · [doi](#)

13. **Quaternary Logic Lookup Table in Standard CMOS**  
D. Brito, **T. Rabuske**, J. Fernandes, P. Flores and J. Monteiro · *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 23, no. 2, pp. 306–316, 2015 · [doi](#)
14. **Noise-aware simulation-based sizing and optimization of clocked comparators**  
**T. Rabuske** and J. Fernandes · *Analog Integrated Circuits and Signal Processing*, vol. 81, no. 3, pp. 723–728, 2014 · [doi](#)
15. **Comparator-based binary-search ADC architectures for UWB receivers**  
**T. Rabuske**, F. A. Rabuske, J. Fernandes, C. Rodrigues and D. Brito · *Analog Integrated Circuits and Signal Processing*, vol. 77, no. 3, pp. 471–482, 2013 · [doi](#)
16. **A 5 MSps 8-bit SAR ADC with single-ended or differential input**  
**T. Rabuske**, C. Rodrigues and S. Nooshabadi · *Microelectronics Journal*, vol. 43, no. 10, pp. 680–686, 2012 · [doi](#)
17. **A 54.2  $\mu$ W 5 MSps 9-bit ultra-low-energy analog-to-digital converter in 180 nm technology**  
**T. Rabuske**, S. Nooshabadi and C. Rodrigues · *Analog Integrated Circuits and Signal Processing*, vol. 72, no. 1, pp. 37–46, 2011 · [doi](#)

## CONFERENCE PAPERS

---

1. **Stacked Ring Oscillators with Fractional Injection Lock**  
G. Rodrigues, R. Borralho, **T. Rabuske** and J. Fernandes · *IEEE International Symposium on Circuits and Systems (ISCAS)*, 2025 · [doi](#)
2. **A Small-Area Current-Mode Input  $\Sigma\Delta$  Modulator for Under-the-Sensors ADC Arrays**  
H. I. Busse, **T. Rabuske**, M. Silva, G. Rodrigues, D. M. Caetano, M. B. Santos and J. Fernandes · *Conference on Design of Circuits and Integrated Systems (DCIS)*, 2024 · [doi](#)
3. **An On-Chip Clock Generation Circuit for Smart Catheters**  
D. Brito, J. Silva, G. Rodrigues, A. Pinto, J. Fernandes and **T. Rabuske** · *IEEE International Symposium on Circuits and Systems (ISCAS)*, 2021 · [doi](#)
4. **A Temperature-Compensated 57 ppm/ $^{\circ}$ C 10 MHz, 2.4  $\mu$ W Stacked Ring Oscillator**  
G. Rodrigues, D. Brito, H. I. Busse, J. Fernandes, J. Silva and **T. Rabuske** · *IEEE International Symposium on Circuits and Systems (ISCAS)*, 2021 · [doi](#)
5. **Towards a Wireless System that Can Monitor the Encapsulation of mm-sized Active Implants in vivo for Bioelectronic Medicine**  
G. Rodrigues, M. Neca, J. Silva, D. Brito, **T. Rabuske**, J. Fernandes, R. Mohrlök, C. Jeschke, J. Meents, K. Nanbakhsh and V. Giagka · *IEEE EMBS Conference on Neural Engineering (NER)*, 2021, pp. 981–984 · [doi](#)
6. **A Biomedical Imaging System Based on an Integrated Array of Magnetoresistive Sensors**  
**T. Rabuske**, M. Silva, D. Brito et al. · *IEEE International New Circuits and Systems Conference (NEWCAS)*, 2021, pp. 1–4 · [doi](#)
7. **Methods for Fast Characterization of Noise and Offset in Dynamic Comparators**  
J. Silva, D. Brito, G. Rodrigues, **T. Rabuske**, A. C. Pinto and J. Fernandes · *IEEE International New Circuits and Systems Conference (NEWCAS)*, 2021, pp. 1–4 · [doi](#)
8. **Polymath: A Platform for Rapid Application Development of Modular EDA Tools**  
**T. Rabuske** · *IEEE International Symposium on Circuits and Systems (ISCAS)*, 2020, pp. 1–5 · [doi](#)

9. **A Sub- $\mu$ W 3–10 MHz Stacked Oscillator with a Duty-Cycle Calibrated Level Shifter**  
G. Rodrigues, D. M. Caetano, D. Brito, J. Fernandes and **T. Rabuske** · *IEEE International Symposium on Circuits and Systems (ISCAS)*, 2020, pp. 1–5 · [doi](#)
10. **Injection Locked Oscillators with Current Reuse**  
M. Benido, **T. Rabuske** and J. Fernandes · *IEEE International Symposium on Circuits and Systems (ISCAS)*, 2019, pp. 1–4 · [doi](#)
11. **A Small-Footprint Quasi-Passive 1st-Order  $\Sigma\Delta$  Modulator**  
G. Rodrigues, J. Fernandes and **T. Rabuske** · *IEEE International Symposium on Circuits and Systems (ISCAS)*, 2019, pp. 1–5 · [doi](#)
12. **A 125 MS/s 10.4 ENOB 10.1 fJ/conv-step Multi-Comparator SAR ADC with Comparator Noise Scaling in 65 nm CMOS**  
S. Liu, J. Paramesh, L. Pileggi, **T. Rabuske** and J. Fernandes · *ESSCIRC*, 2018, pp. 22–25 · [doi](#)
13. **Tunable k $\Omega$  to G $\Omega$  pseudo-resistor with bootstrapping technique**  
D. M. Caetano, D. Oliveira, J. Silva, **T. Rabuske** and J. Fernandes · *IEEE International Midwest Symposium on Circuits and Systems (MWSCAS)*, 2017, pp. 1569–1572 · [doi](#)
14. **Variable Bandwidth Chopper Amplifier for Eddy-Current Non-Destructive Testing**  
J. Silva, D. Oliveira, D. M. Caetano, J. Fernandes and **T. Rabuske** · *International Workshop on Electromagnetic Nondestructive Evaluation (ENDE)*, 2016
15. **A 12-Bit SAR ADC with Background Self-Calibration Based on a MOSCAP-DAC with Dynamic Body-Biasing**  
**T. Rabuske** and J. Fernandes · *IEEE International Symposium on Circuits and Systems (ISCAS)*, 2016 · [doi](#)
16. **Fast settling VGA for eddy-currents non-destructive testing with an array of magneto-resistors**  
D. M. Caetano, F. A. Rabuske, D. Oliveira, **T. Rabuske** and J. Fernandes · *Conference on PhD Research in Microelectronics and Electronics (PRIME)*, 2016 · [doi](#)
17. **A 9-b 0.4-V charge-mode SAR ADC with 1.6-V input swing and a MOSCAP-only DAC**  
**T. Rabuske** and J. Fernandes · *ESSCIRC*, 2015, pp. 311–314 · [doi](#)
18. **An efficient RF power harvester for low input power with reduced dead-zone**  
H. Gonçalves, J. Fernandes, **T. Rabuske** and M. Martins · *IEEE International Symposium on Circuits and Systems (ISCAS)*, 2014 · [doi](#)
19. **Quadrature relaxation oscillator with FoM of –165 dBc/Hz**  
E. Ortigueira, **T. Rabuske**, L. B. Oliveira, J. Fernandes and M. M. Silva · *IEEE International Symposium on Circuits and Systems (ISCAS)*, 2014 · [doi](#)
20. **A sub-ranging 2-step 7-bit self-calibrated comparator-based binary-search ADC**  
F. A. Rabuske, **T. Rabuske** and J. Fernandes · *IEEE International Symposium on Circuits and Systems (ISCAS)*, 2014 · [doi](#)
21. **A self-calibrated 10-bit 1 MSps SAR ADC with reduced-voltage charge-sharing DAC**  
**T. Rabuske**, J. Fernandes, F. A. Rabuske, C. Rodrigues and M. B. Santos · *IEEE International Symposium on Circuits and Systems (ISCAS)*, 2013, pp. 2452–2455 · [doi](#)
22. **A 5-bit 1.5 GSps calibration-less binary-search ADC using threshold-reconfigurable comparators**  
**T. Rabuske**, F. A. Rabuske, J. Fernandes and C. Rodrigues · *IEEE International Symposium on Circuits and Systems (ISCAS)*, 2013 · [doi](#)

23. **An IR-UWB transmitter with digital pulse duration control**

D. Correia, M. dal Alba, M. A. Martins, **T. Rabuske**, C. Rodrigues and J. Fernandes · *IEEE International Symposium on Circuits and Systems (ISCAS)*, 2012, pp. 233–236 · [doi](#)

24. **PyCO: A parallel genetic algorithm optimization tool for analog circuits**

**T. Rabuske**, R. Pinheiro, J. Fernandes and C. Rodrigues · *IEEE International Symposium on Circuits and Systems (ISCAS)*, 2012 · [doi](#)

25. **A 749 nW 1 MSps 8-bit SAR ADC at 0.5 V employing boosted switches**

**T. Rabuske**, J. Fernandes, S. Nooshabadi, C. Rodrigues and F. A. Rabuske · *IEEE International Conference on Electronics, Circuits and Systems (ICECS)*, 2012 · [doi](#)

26. **A 4-bit 1.5 GSps 4.2 mW comparator-based binary-search ADC in 90 nm**

**T. Rabuske**, F. A. Rabuske, J. Fernandes and C. Rodrigues · *IEEE International Conference on Electronics, Circuits and Systems (ICECS)*, 2012 · [doi](#)

27. **A track-and-hold for single-ended or differential input with adjustable output common mode**

**T. Rabuske**, C. Rodrigues and S. Nooshabadi · *IEEE International Midwest Symposium on Circuits and Systems (MWSCAS)*, 2011 · [doi](#)

28. **An energy-efficient 1 MSps 7  $\mu$ W 11.9 fJ/conversion-step 10-bit SAR ADC in 90 nm**

**T. Rabuske**, C. Rodrigues and S. Nooshabadi · *IEEE International Symposium on Circuits and Systems (ISCAS)*, 2011

29. **A novel energy-efficient digital controller for charge-sharing successive-approximation ADCs**

**T. Rabuske**, F. A. Rabuske and C. Rodrigues · *IEEE Latin American Symposium on Circuits and Systems (LASCAS)*, 2011

30. **Distributed version control as a tool to increase productivity in analog and mixed-signal design**

R. Pinheiro, **T. Rabuske** and C. Rodrigues · *Iberchip*, 2011

31. **An energy-efficient successive-approximation register analog-to-digital converter in 180 nm**

**T. Rabuske** and S. Nooshabadi · *IEEE Asia Pacific Conference on Circuits and Systems (APCCAS)*, 2010 · [doi](#)

## PATENTS

---

[W02021125987](#)

“Method for detection and classification of non-periodic signals and the respective system that implements it,” 2021. Granted

Filed

6 further applications under examination.

## SERVICE & COMMUNITY

---

2024 – Present

### Senior Member

Institute of Electrical and Electronics Engineers (IEEE)

Elevated grade, held by a minority of IEEE members and requiring demonstrated professional maturity and significant performance in the field.

2018 – Present

**Member, Analog Signal Processing Technical Committee**

IEEE Circuits and Systems Society

Review and programme work in analog signal processing for CASS conferences and transactions.

2017 – 2023

**Member, Scientific Council**

INESC-ID, Lisbon

Ongoing

**Reviewer**

IEEE Journal of Solid-State Circuits, Transactions on Circuits and Systems I and II, Transactions on VLSI Systems, and CASS conferences.

## **AWARDS & HONOURS**

---

**2018, 2019**

Finalist, INESC-ID Best Young Researcher Award

**2016**

PhD awarded with merits and honours, Instituto Superior Técnico, Universidade de Lisboa

**2016**

Finalist, Prof. Abreu Faro Prize for the best PhD thesis of Universidade de Lisboa

**2015, 2016**

Finalist, INESC-ID Best PhD Candidate Award

**2016**

Most-downloaded paper of the month, IEEE Journal of Solid-State Circuits – and 49th most downloaded across IEEE Xplore, June 2016

## **ADVISING & INVITED TALKS**

---

Advised/Co-advised six doctoral candidates and six MSc students at Instituto Superior Técnico and INESC-ID, 2017 – 2023.

2019

“Designing ADCs for the IoT: Architectures, Techniques and Tools,” IEEE Seasonal School on Circuits and Systems for IoT

2019

“Projeto de ADCs para a Internet das Coisas,” IEEE CASS Tech Talk, UFPel