

Taimur Rabuske

Analog and mixed-signal IC design · architecture to silicon

taimur.rabuske@gmail.com · Wilmington, Massachusetts, USA · [LinkedIn](#) · [Google Scholar](#)

PROFILE

Analog and mixed-signal IC designer with a PhD in microelectronics and more than fifteen years of CMOS silicon experience. Own subsystems from feasibility and architecture through transistor-level design, verification and silicon validation. Work spans data converters, clocking, power management and high-speed links, with tape-outs across eight process generations from 0.5 μm to 5 nm. Combine circuit design with an MSc in computer science, Python-based EDA tooling and research leadership.

EXPERIENCE

2023 – Present

Analog/Mixed-Signal Design Engineer

Analog Devices · Wilmington, Massachusetts

- Own analog and mixed-signal subsystems from feasibility, architecture exploration and specification through implementation, verification, validation and silicon bring-up support.
- Delivered LDOs, clock-synthesis circuits, a die-to-die SerDes link and an audio $\Sigma\Delta$ ADC, including converter cores, sampling networks, comparators, references and biasing.
- Develop new subsystem architectures; six patent applications are under examination.
- Advanced-node FinFET and SOI design, with noise, matching, settling and jitter budgets for high-resolution converters and their clocking.

2016 – 2023

Senior Researcher

INESC-ID · Lisbon, Portugal

- Led analog and mixed-signal research in low-power SAR and charge-sharing ADCs, $\Sigma\Delta$ modulators, comparators and calibration, clock generation, and biomedical and sensor front-ends.
- Delivered research prototypes from specification and architecture through schematic, custom layout, DRC/LVS sign-off, tape-out, PCB, firmware and bench characterisation, in 0.35 μm to 40 nm processes.
- Defined system specifications across silicon, board and software; led biomedical and industrial programmes and designed circuits for industry partners' commercial products.
- Supervised and co-supervised six doctoral and six MSc researchers, wrote funding proposals, and served on the Scientific Council (2017–2023).

2010 – 2016

Research Assistant

INESC-ID · Lisbon, Portugal

Charge-sharing SAR ADC research: MOSCAP-based DACs, comparator offset auto-zeroing and self-timed control, validated in four fabricated prototypes.

Visiting Scholar · Delft University of Technology · Delft, Netherlands · 2018

Intern Researcher · Gwangju Institute of Science & Technology · Gwangju, South Korea · 2009

TECHNICAL EXPERTISE

Circuits

- SAR, charge-sharing, $\Sigma\Delta$ and high-speed flash ADCs; comparators and calibration
- Clock synthesis; LC, ring, relaxation and injection-locked oscillators
- LDOs, references and biasing; die-to-die SerDes; biomedical and sensor front-ends

Design flow

- Architecture and specification; behavioural modelling; noise, settling and jitter budgets
- PVT and Monte Carlo verification; custom layout, DRC/LVS/PEX and tape-out
- System integration, PCB and firmware development, bring-up and bench characterisation

Software & tools

- Cadence Virtuoso and Spectre; HSPICE; Python modelling, optimisation and test automation
- gm/ID sizing and EDA tools; SystemVerilog RTL, synthesis and digital sign-off when needed
- Version control and continuous integration for analog and mixed-signal teams

Silicon: 0.5 μm · 0.35 μm · 0.18 μm · 0.13 μm · 65 nm · 40 nm · 22 nm · 5 nm · bulk CMOS, SOI and FinFET.

EDUCATION

2012 – 2016

PhD, Electrical and Computer Engineering (with honors)

Instituto Superior Técnico, Universidade de Lisboa

Microelectronics; charge-sharing SAR ADCs. Thesis published as a Springer monograph.

2010 – 2011

MSc, Computer Science

Universidade Federal de Santa Maria, Brazil

2005 – 2009

BSc, Electrical Engineering

Universidade Federal de Santa Maria, Brazil

SELECTED RESEARCH & RECOGNITION

Senior Member, IEEE · 2024 – Present.

Advised/Co-advised six doctoral candidates and six MSc students at Instituto Superior Técnico and INESC-ID, 2017 – 2023.

Book: Charge-Sharing SAR ADCs for Low-Voltage Low-Power Applications. T. Rabuske and J. Fernandes · Analog Circuits and Signal Processing series · Springer, Cham, 2017. [doi](#)

1. A SAR ADC With a MOSCAP-DAC

T. Rabuske and J. Fernandes · *IEEE Journal of Solid-State Circuits*, vol. 51, no. 6, pp. 1410–1422, 2016. Most-downloaded JSSC paper, June 2016 · [doi](#)

Patents: 1 granted; 6 further applications under examination.

Languages: English – fluent · Portuguese – native.

Full professional record and publications: taimurrabuske.com/cv/